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A Novel 1-Phase Switched-attached-Inductor DC–AC Inverter for Solar Arrangement

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Abstract

This paper exhibits another single-stage switched coupled-inductor DC– AC inverter highlighting higher voltage picks up than the current single-stage q-Z-source and semi-Z-source inverters. Like semi-Z-source inverters, the proposed inverter can obtain higher output than input voltage. The proposed inverter also shares a common ground between DC input voltage and AC output voltage. Thus, possible ground leakage current problem in non-isolated grid-tied inverters can be eliminated with the proposed inverter. A 120 W prototype inverter is built and tested to verify the performance of the proposed inverter. A hypothetical examination of the proposed inverter is depicted and a 280-W trial model is worked to check the execution of the inverter.

I. INTRODUCTION

These days, there is an expanding interest for ease single-stage dc– ac inverters in numerous applications, for example, photovoltaic (PV), energy component, and battery controlled frameworks. The ordinary techniques are appeared in Fig. 1. Fig. 1(a) demonstrates the surely understood full-connect (FB) inverter alluded to as buck inverter in this paper [1]– [3]. In this circuit, the inverter yield voltage (vo) can't be more prominent than input voltage (Vin). At the point when the info voltage is low, a lift dc– dc converter is embedded between Vin what's more, the inverter connect as appeared in Fig. 1(b). Be that as it may, the two topologies in Fig. 1 have distinctive info and yield grounds.

This may bring about huge spillage current in applications, for example, transformer-less network tied PV inverter, which will cause security also, electromagnetic obstruction issue [4]– [7]. So as to beat the hindrances of the ordinary inverters, a substantial number of single-organize inverters are proposed [8], [9]. What's more, the Z-source inverter topologies survive the impediments said before [10]–[10]. Fig. 2(a) demonstrates the present bolstered (CF) single-stage q-Z-source inverter [13], and Fig. 2(b) is the semi-qZ-source inverter with dc– dc support converter. Which is an enhanced variant of Fig. 2(a) both the inverters have a similar voltage pick up as appeared underneath and require as it were two dynamic changes to get a similar most extreme voltage pick up as the FB inverter appeared in Fig. 1(a) in (1), D is characterized as the obligation proportion of switch S2. As

appeared in Fig. 2, the two topologies share regular grounds amongst Vin and Vo, along these lines they can limit the conceivable ground spillage current issue viably [7] when they are utilized for PV inverter. Be that as it may, as delineated in Fig. 2(c), their feasible most extreme voltage pick up is restricted to 1, which implies that they are not reasonable for applications where input voltage is low. With a specific end goal to beat the impediments of Fig. 2 while keeping up the doubly ground includes, a three-switch three-state single-stage Z-source inverter (TSTS-ZSI) was presented in [13].

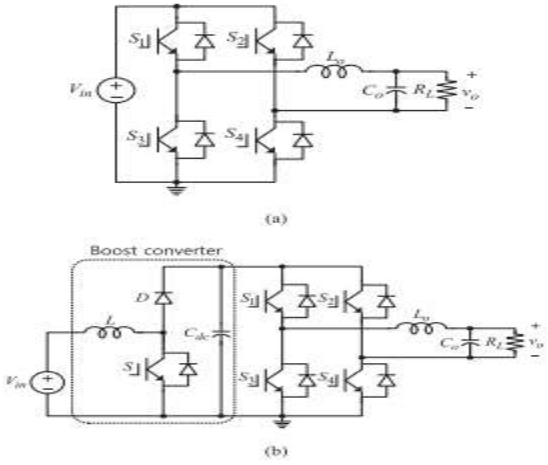

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Fig. 1 Regular single-stage inverters (a) FB inverter (b) FB inverter

$$\frac{v_o}{V_{in}} = \frac{2D - 1}{D}.$$

Fig. 3 demonstrates the lift based TSTS-ZSI and buck-boost based TSTS-ZSI, separately. The inverters can have higher voltage pick up than 1, and they include three switches, three capacitors, and three inductors.

Inverter (b) Semi-q-Z-source inverter (c) Voltage pick up. Albeit higher voltage pick up is acquired, the three inductors (L1, L2, and L3) in the TSTS-ZSI make the circuit somewhat cumbersome also, substantial. Moreover, the switch signs of the inverter are all extraordinary and generally convoluted. In this paper, a solitary stage exchanged coupled-inductor DC– AC inverter is proposed. Like the TSTS-ZSIs, the proposed inverter can acquire higher voltage pick up than the circuits in Fig. 2 what's more, keeps up same ground amongst Vin and Vo.

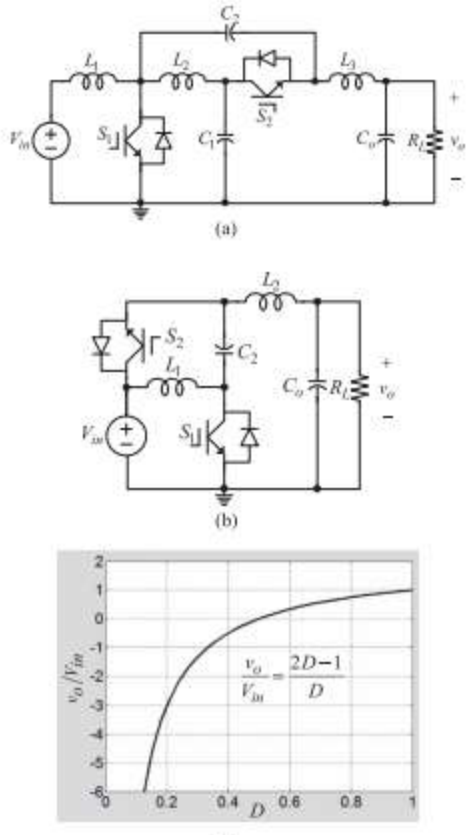

Fig. 2 Single-stage q-Z-source inverters (a) Single-stage CF-q-Z-source

The proposed inverter likewise requires three dynamic switches, however every one of the inductors in the circuit can be coupled together, which will prompt more conservative and financially savvy arrangement than the TSTS-ZSI. Moreover, the switch flag age is moderately less difficult than the TSTS-ZSI. A 280-W model inverter is assembled and its exhibitions are checked through examination.

II. TASK PRINCIPLE OF THE PROPOSED DC– AC INVERTER

Fig. 4 demonstrates the proposed inverter and it takes comparative structure with the single-stage CF-q-Z-inverter appeared in Fig. 2(a). Contrasted and Fig. 2(a), the proposed inverter has an extra switch (Sx), capacitor (Cx), and inductor (L2) coupled with inductor L1. The inductors L1 and L2 are combined with 1: n turn's proportion and every one of the

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inductors in the proposed topology can be coupled by and large as will be examined in Section III. The additional 1: n coupled inductor adds to the expansion of voltage pick up. In spite of the fact that the spillage inductance of the coupled inductor may actuate a voltage spike crosswise over switch S1, this is definitely not a noteworthy issue on the grounds that such a voltage spike and the voltage of S1 are low. In Section III, it will be discovered that the voltage worry of S1 is continuously 50% of S2 or Sx if spillage inductance isn't considered.

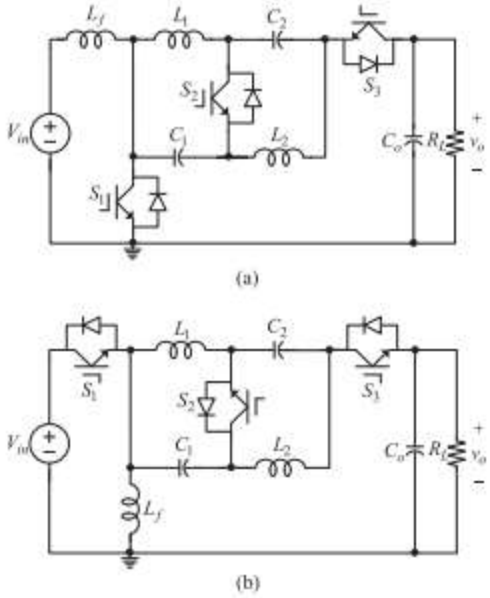

Fig. 3 Three-switch TSTS-ZSI [17]. (a) Boost-based TSTS-ZSI. (b) Buck-help based TSTS-ZSI.

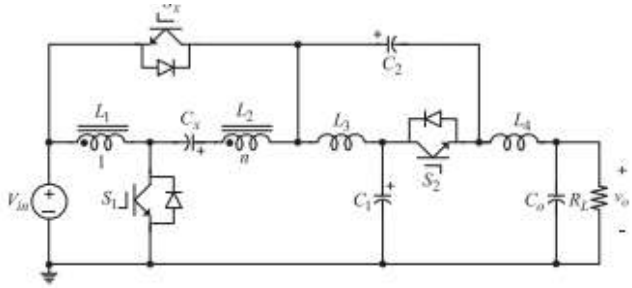

Fig. 4 Proposed dc– ac inverter

In this manner, as long as the voltage overshoot caused by the spillage inductance isn't so high, the voltage worry of S1 will be not exactly that of S2 and there isn't much issue in choosing exchanging gadget for S1. Then again, the spillage inductance is helpful in constraining the present going through Cx. Switches S1 and S2 are reciprocal as in the single-stage qZ-source inverter and the switch Sx is synchronized with S1.

A. Mode Analysis of the Proposed Inverter

Fig. 5 indicates task of the proposed inverter and there are two operational modes amid one exchanging cycle. In mode 1, switches S1 and Sx are turned-ON, and S2 is killed. In mode 2, switches S1 and Sx are killed, and S2 is turned-ON. Followings are the clear mode investigation of the proposed inverter. In mode 1, the capacitor Cx is charged to (n + 1) Vin. Since the Cx is being charged and released amid one exchanging Period, its voltage has swell and the swell voltage relies upon the yield control. In this way, when the voltage distinction between (n + 1)Vin and Cx is high, generally high flood (charging) current will course through Vin − Dx (Sx) − L2 − Cx − S1 and the exchanging gadgets in this way (Sx and S1) can be harmed.

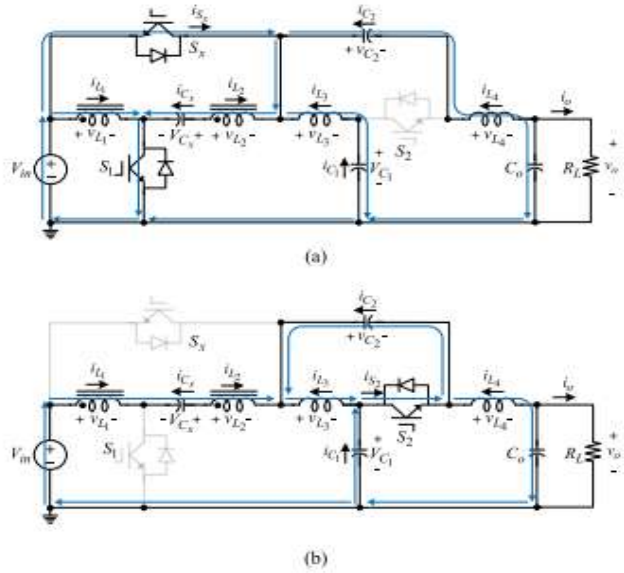

Fig. 5 Mode examination of the proposed inverter (a) Mode 1: S1 and Sx are ON, and S2 is OFF. (b) Mode 2: S1 and Sx are OFF, and S2 is ON.

With a specific end goal to confine the high flood current, a current restricting inductor is vital. In this paper, the spillage inductance created by the coupling of L1 and L2 fills in as the present restricting inductor. From Fig. 5(a), the voltage and current relations in mode 1 are inferred as

$$VCx = Vin + vL2 = (n + 1)\,Vin \qquad (2)$$

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$$\begin{cases} vL1 = Vin \\ vL3 = Vin - VC1 \\ vL4 = Vin - vC2 - vo \end{cases} \quad (3)$$

$$\begin{cases} iC1 = iL3 \\ iC2 = iL4 \\ iCx = iin - iL1 + iL3 + iL4 \end{cases} \quad (4)$$

In mode 2, capacitor Cx is released by the inductor current, iL1. From Fig. 5(b), the voltage and current relations in mode 2 are inferred as takes after:

$$\begin{cases} (1 + n)\, vL1 = Vin + VCx - vC2 - VC1 \\ vL3 = vC2 \\ vL4 = VC1 - vo \end{cases} \quad (5)$$

$$\begin{cases} iC1 = -iL1 - iL4 \\ iC2 = -iL1 - iL3 \end{cases}$$

$$iCx = -iL1\ . \quad (6)$$

From the aforesaid equations, voltage relations are derived as follows:

$$VC1 = vC2 + vo \quad (7)$$

$$VC1 = (n + 2)\, Vin. \quad (8)$$

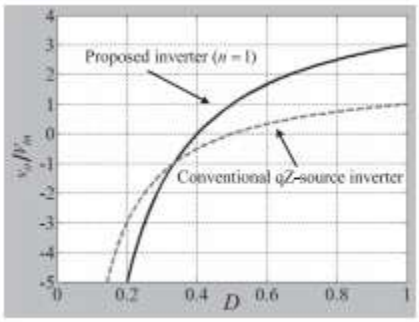

Fig. 6 Voltage gain comparison.

From the flux (volt–second) balance condition on L3, the capacitor C2 voltage is derived as follows:

$$v_{C_2} = \frac{(1-D)(n+1)}{D} V_{\text{in}}$$

Where D is the duty cycle of switch S2 By using (7)–(9), the voltage gain of the proposed inverter is derived as follows:

$$\frac{v_o}{V_{\text{in}}} = \frac{(2n+3)(2D-1)+1}{2D} \le n+2.$$

Fig. 6 demonstrates the voltage pick up of the proposed inverter when n = 1 and contrasted and the regular inverters appeared in Fig. 2. It is discovered that the proposed inverter has a higher voltage pick up than the customary inverters appeared in Figs. 1(a) and 2. As per the charge adjust condition on Cx, C1, and C2, the inductor streams arrived at the midpoint of in one exchanging period are inferred as takes after:

$$iL_{1avg} = \frac{(2d\text{-}1)(n+1)\, i_0}{D} \quad (11)$$

$$iL2.\ avg = 0 \quad (12)$$

$$iL3.\ avg = iL4\ .\ avg = -io \quad (13)$$

$$iS2.\ avg = iSx\ .\ avg = io\ . \quad (14)$$

Streams of inductors L1 and L2 are distinctive in separate mode not at all like inductor streams iL3 and iL4. In mode 1, where current swell is disregarded, they are determined

$$i_{L_1} = \frac{(2D-1)(n+1-D)}{D(1-D)} i_o$$

$$i_{L_2} = -\frac{(2D-1)}{(1-D)} i_o.$$

In mode 2, they are expressed as follows:

$$i_{L_1} = i_{L_2} = \frac{2D-1}{D} i_o.$$

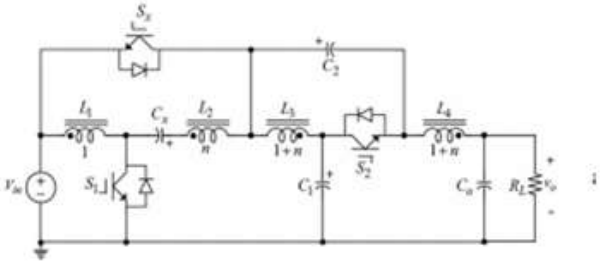

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Fig. 7 Circuit topology of the proposed inverter when all inductors are coupled into one center

B. Tweak Scheme of the Proposed Inverter

Modulation plan of the proposed inverter is the same as that of the single-stage q-Z-source inverter. By characterizing the yield voltage of the inverter as (18), tweak record (M) of the inverter is determined as takes after:

$$vo = Vm \sin \omega t \quad (18)$$

$$M = Vm / Vin \quad (19)$$

By substituting (18) and (19) into (10), the accompanying obligation cycle condition is determined as takes after:

$$D = \frac{n+1}{2n+3-M\sin(\omega t)}, \ (0 \le M \le n+2).$$

When n = 1 and M = 3, the duty cycle range of the proposed inverter is 0.25–1.0. Fig. 7 represents the gate signal generation of the proposed inverter. When reference signal (vref) is greater than the carrier signal (vc), switch S2 is turned on and switch S1 is turned OFF.

III. MAGNETIC INTEGRATION OF INDUCTORS AND COMPARISON

A. Magnetic Integration of Inductors

As discussed in Section II, the L1 and L2 are coupled with 1: n ratio to obtain higher voltage gain. In this section, it is revealed that all the four inductors (L1, L2, L3, and L4) in the proposed inverter can be coupled using one magnetic core.

TABLE I

DEVICE STRESS OF THE PROPOSED INVERTER

	Voltage stress	Current stress
S_1	$\frac{2n+3+M}{2M}V_o$	$\frac{(2n+3-M)(M-1)}{n+2-M}I_o$
S_2	$\frac{2n+3+M}{M}V_o$	$\frac{2n+3+M}{n+1}I_o$
S_x	$\frac{2n+3+M}{M}V_o$	$\frac{2n+3-M}{n+2-M}I_o$

B. Examination of Switch Stress and Others

From Fig. 5 and (8), (9), voltage worries of the three switches can be resolved. Also, the switch current stresses can be resolved from (4), (6), (13)) and Fig. 5. Table I demonstrates greatest switch worry of the proposed inverter. Table II thinks about the proposed inverter when n = 1 with the help based TSTS-ZSI appeared in Fig. 3(a). k is greatest of balance file.

In spite of the fact that the buck– support based TSTS-ZSI has bring down gadget stresses, it has downsides like more muddled door flag age, irregular information and yield current, and requires extra LC channel that manufactures the circuit structure more unpredictable furthermore, extensive inductor. Hence, the lift based TSTS-ZSI is contrasted and the proposed inverter. From the consequence of Table II, it is clear that the general voltage what's more, current worries of the proposed inverter are more prominent than those of the TSTS-ZSI and the proposed inverter requires one more capacitor. Notwithstanding, current worry of the proposed inverter is lower than that of the lift based TSTS-ZSI when M is lower than 2.4. In addition, the proposed inverter can lessen the attractive volume through the coupling of every single separate inductor.

Correlation of most extreme current swell, normal current, also, most extreme capacitor voltage is outlined in Table II. Concurring to the Table II, when contrasted and the lift based TSTS-ZSI, the inductor current swells of the proposed inverter are diminished by more than 2 because of coupling impact. In Table II, L1 and L3 of the proposed inverter are self-inductances of the coupled inductor. Likewise, self-inductances L1 and L2 of the proposed inverter are the same and L3 and L4 are likewise the same when all inductors are combined with n = 1. The boost based TSTS-ZSI is accepted that L1 and L2 are equivalent. In spite of the fact that, the C2 capacitor voltage of the proposed inverter is more noteworthy than that of the lift based TSTS-ZSI, the capacitor voltages of Cx and C1 in the proposed converter are lower than those of the lift based TSTS-ZSI. In addition, inductor has more effect on size and weight than capacitor. The normal inductor streams of the proposed inverter and lift based TSTZ-ZSI in one exchanging period are nearly the same. All in all, the proposed inverter can decrease by and large attractive volume since bring down inductance is required. Furthermore, the lift based TSTS-ZSI ought to have expansive yield capacitor

TABLE II

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ELECTRICAL SPECIFICATIONS OF THE PROPOSED INVERTER

Output power		280 W
Input voltage		62 Vdc
Output voltage		110 Vrms / 60 Hz
Switching frequency		20 kHz
IGBT (S_x, S_1, S_2)		FGH40N60
Coupled inductor	Core	EE7066
	Inductance (L_1, L_2)	60 uH
	Inductance (L_3, L_4)	240 uH
Capacitance (C_x, C_1)		100 uF
Capacitance (C_o)		4.4 uF

As a result of irregular yield current. In addition, the entryway flag age of the proposed inverter is significantly less complex than that of the TSTS-ZSI.

IV. EXPERIMENT RESULTS

A 280-W model inverter is manufactured and tried. Point by point electrical details of the proposed inverter are abridged in Table II. As of now said in Section II, a moderately little present constraining inductor is required in the way Vin − Dx (Sx) − L2 − Cx − S1 to restrain the high flood current. In the proposed circuit, the spillage inductance (around 300 nH) produced by

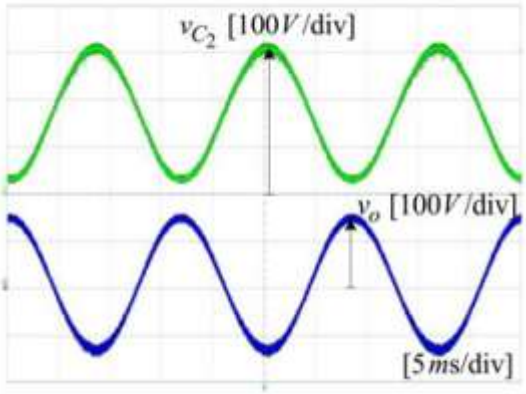

Fig. 8 Test waveforms of the proposed inverter (vC 2, vo)

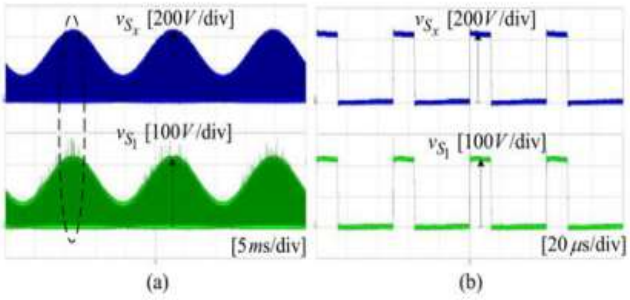

Fig. 9 Test waveforms of the proposed inverter (vSx, vS1) (a) Switching waveform. (b) Zoomed-in waveform of (a).

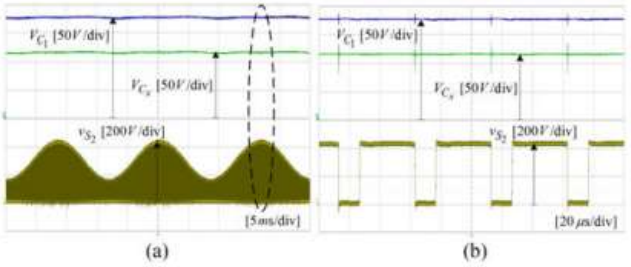

Fig. 11 Test waveforms of the proposed inverter (vS2, VC 1, VC x) (a) Switching waveform (b) Zoomed-in waveform of (a).

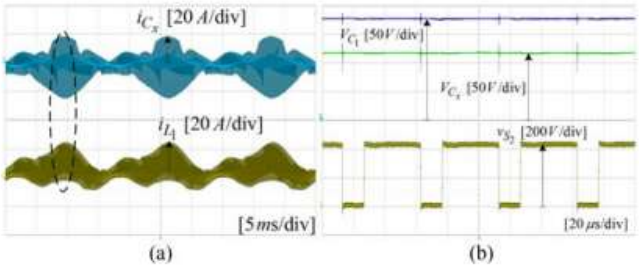

Fig. 12 Test waveforms of the proposed inverter (a) Current waveforms (iL1, iC x). (b) Zoomed-in waveform of (a). Coupling of L1 and L2 is utilized for this reason. Followings

Are the test waveforms of the proposed inverter when Vin = 62 V, M = 2.5, and Po = 280 W. Fig. 9 demonstrates the test waveform of the yield voltage furthermore, the capacitor C2 voltage. Figs. 10 and 11 demonstrate the voltages over all switches (vSx, vS1, and vS2). Of course, there is

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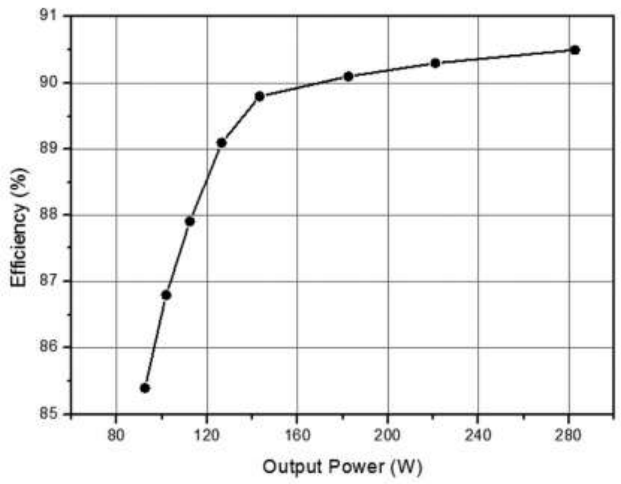
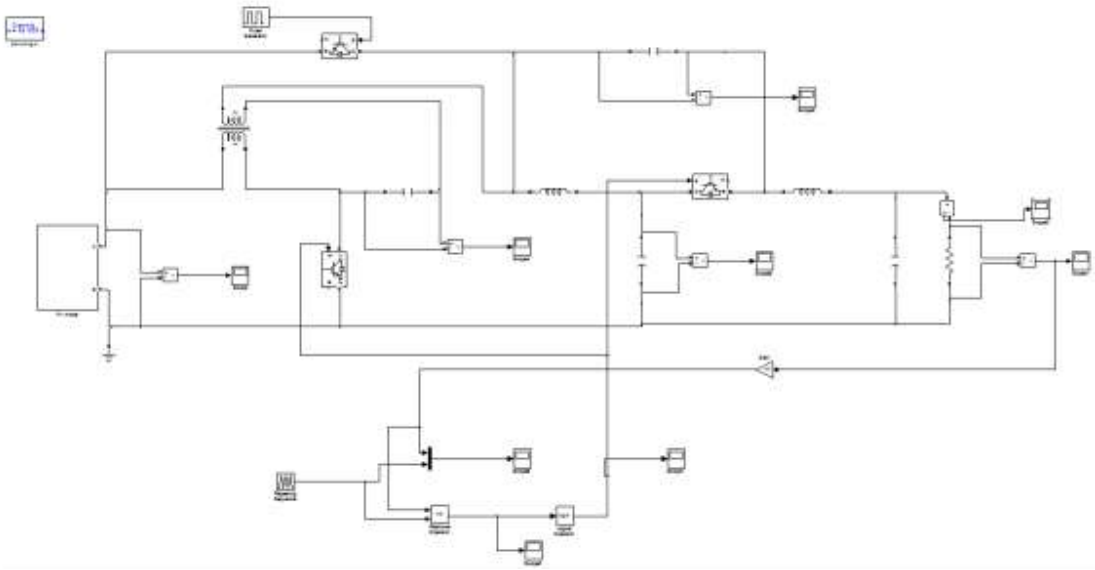


Fig. 14 Proficiency of the proposed inverter

voltage overshoot in switch S1 caused by the spillage inductance what's more, there are no discernible overshoots in the switches S2 voltage fluctuating with D, the voltages crosswise over C1 and Cx are nearly consistent and they are settled to 3Vin and 2Vin , individually. Figs. 12 and 13 indicate current waveforms. Demonstrates the effectiveness of the proposed inverter tried with Vin = 62 V with yield control fluctuates.

SIMULATION MODEL



SIMULATION RESULTS

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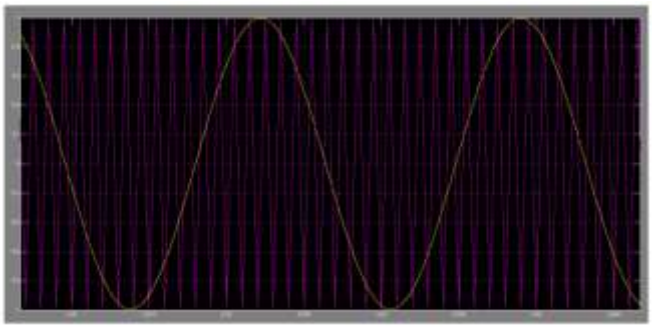

Fig.1 Gate signal generation of the proposed inverter

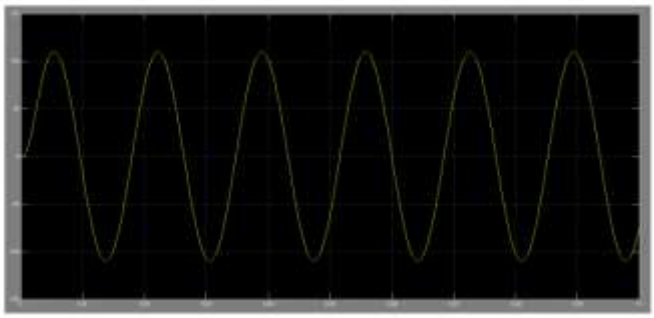

Fig.2 Simulation waveforms of the proposed inverter (vC 2, vo)

V. CONCLUSION

In this paper, the single-stage exchanged coupled inductor dc–ac inverter was exhibited. It has an activity standard comparable to that of a solitary stage q-Z-source inverter. With the expansion of parts Sx, Cx, and the coupled inductor, voltage pick up of the proposed inverter can be stretched out to more noteworthy than 2. The attractive incorporation of all inductors diminishes the converter volume essentially and the

Proposed inverter has moderately basic entryway flag age. Also, like the single-stage q-Z source inverter and the TSTS-ZSI, the proposed inverter shares normal grounds between the dc input and the air conditioner yield voltage. A 280-W model inverter was manufactured and tried to check activity of the proposed inverter.

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